Remarks

Applicant affirms that in response to the requirement for election of species for examination purposes, his attorney elected Group I, Claims 1 to 18 and 21, with traverse. Applicant understands that all of the claims will be examined when a generic claim is allowed.

Claims 14 and 15 were objected to under 37 CFR 1.75(c) as being of improper dependent form. Section 1.75(c) of 37 CFR deals primarily with multiple dependent claims. Claims 14 and 15 are not multiple dependent claims as they each refer back to only one claim. Applicant can find nothing in 37 CFR 1.75(c) that prohibits the form of Claim 14 or 15. These are common types of claims that appear in many issued patents.

Claims 12 and 13 were rejected under 35 U.S.C. 112, second paragraph "as indefinite because they are method claims dependent upon apparatus claim 1." Again, it is common practice to have this type of claim and Applicant can cite a number of patents where this is done. Applicant respectfully requests that the Examiner either withdraw this rejection or cite a section of 37 CFR or the MPEP that specifically prohibits this type of claim.

Claims 1 to 18 were rejected under 35 U.S.C. 103(a) as unpatentable over Dingwall in view of Yamauchi et al. ("Yamauchi"). Dingwall is cited to show a complementary source follower circuit but, as the Examiner notes, "does not show a back bias control circuit coupled to the back gate terminals of the transistors for

controlling the threshold voltage of the transistors in active and standby modes as called for in claims 1 and 16."

Yamauchi shows a CMOS inverter, not a source follower circuit. The Examiner cites Yamauchi to show a back bias control circuit, referring to Figure 1C. In Figure 1C of Yamauchi, voltage is applied to "Vcc" of the PMOS transistor for the standby mode ("/ACT") and voltage is applied to "Veq1" for the active mode ("ACT"). Figure 1B in Yamauchi shows the location of "Vcc" and "Veq1." Yamauchi's "Vcc" is also labeled "Vcc" in Applicant's Figure 11 and Yamauchi's "Veq1" is the back of the transistor, labeled "B" in Applicant's Figure 11. Similarly, in Yamauchi's Figure 1C, voltage is applied to "Vss" of the NMOS transistor for the standby mode, and voltage is applied to "Veq2" for the active mode. Comparing Yamauchi's Figure 1B to Applicant's Figure 11 shows that "Vss" is labeled the same and that "Veq2" in Figure 1B of Yamauchi corresponds to the back "B" of the transistor in Applicant's Figure 11.

In a conventional transistor of a CMOS inverter or a source follower circuit, such as shown by Yamauchi in Fig.1A and Dingwall, respectively, there is a connection from the back of each transistor to the source of the transistor, although normally that connection is not described. If Yamauchi's back bias circuit is applied to the circuit arrangement of Dingwall, as the Examiner suggests, there would still be a connection from the back of each transistor to the source because in Yamauchi the source voltages Vcc and Vss are the same potential as each source. Applicant's claims exclude a signal line connection between the body and the source. Also, in Yamauchi

the purpose of the back bias circuit in active mode is to achieve high speed operation. Applicant's purpose is to achieve linearity in active mode and the references do not teach how to do that or even the desirability of doing that.

Applicant's Claims 1, 16, part (C), (also Claim 19, part (D)) require "a control signal line connection from each of said source terminals to an output terminal." There is no control signal line connection from the source terminals to the output terminal in Yamauchi. Thus, Yamauchi fails to meet this requirement of Applicant's claims. If Yamauchi were combined with Dingwall, the combination would still fail to meet this requirement of Applicant's claims. Applicant's claims therefore effectively distinguish over Yamauchi and the combination of Yamauchi with Dingwall.

Applicant does not agree that it is obvious to "include the Yamauchi et al.'s back bias control circuit in the circuit arrangement of Dingwall." First, Dingwall shows a complementary source follower circuit. In a complementary source follower circuit the sources of the two transistors are connected, as shown in Dingwall's Figure 3 and Applicant's Figure 11. Yamauchi shows a conventional CMOS inverter circuit. In Yamauchi, the drains of the two transistors are connected together, not the sources. This is shown in Yamauchi's Figure 1B and is described in column 4, lines 12 to 18, of Yamauchi. Thus, one cannot simply attach Yamauchi's back bias control circuit to Dingwall. One must first decide whether to re-connect Dingwall's transistors so that the drains are connected, as in Yamauchi, or re-wire Yamauchi so that it is compatible with Dingwall. Doing either one creates other circuit problems that must be solved. It is

therefore not obvious how Yamauchi' circuit could be combined with Dingwall.

Moreover, the purpose of Yamauchi's back bias control circuit is to reduce leakage current in a standby state. Thus, the only incentive to combine Yamauchi's back bias control circuit with Dingwall would be to reduce leakage current in Dingwall's standby state. However, Dingwall expressly states that in his invention "leakage currents ... are negligible." (Column 4, lines 26 to 29.) There is therefore no motivation to use Yamauchi's back bias control circuit in Dingwall and it would therefore not be obvious to do so.

Finally, Dingwall uses a complementary source follower circuit as a voltage divider and Yamauchi is trying to improve operating speed and to reduce leakage in a conventional CMOS inverter. Applicant 's invention is directed at achieving linearity and neither Dingwall, Yamauchi, or any of the other references cited is directed at the problem. There is simply no teaching in these references of how linearity could be achieved and the references are not even concerned with linearity.

Claims 1 to 7, 9 to 18, and 21 were rejected under 35 U.S.C. 103(a) as unpatentable over Taylor in view of Yamauchi. Taylor was cited to show a complementary source follower circuit but "does not show a back bias control circuit coupled to the back gate terminals of the transistors for controlling the threshold voltage of the transistors in active and standby modes." In Taylor's invention, the peak-to-peak voltage swing between Vcc and Vss on the input of the source follower is reduced between Vcc and the threshold voltage of PMOS transistor and the threshold voltage of

NMOS transistor on the output as shown in Fig.3. On the other hand, the peak-to-peak voltage swing on the output of a conventional inverter is substantially the same as on the input. That is, both the input and output voltages typically swing approximately between the rail voltages, Vcc and Vss. This means that the output line of a source follower circuit can reduce consumption power. This is the purpose of Taylor's invention. Taylor, therefore, seems to be equivalent to Dingwall. Yamauchi has been discussed and Applicant's comments concerning Yamauchi in the previous paragraph would apply equally well to this rejection.

Claim 8 was rejected under 35 U.S.C. 103(a) as unpatentable over Taylor in view of Yamauchi. Taylor and Yamauchi have been discussed hereinabove and Applicant has nothing further to add to those comments.

Claims 1 to 7, 9 to 18, and 21 were rejected under 35 U.S.C. 103(a) as unpatentable over IBM-TDB in view of Yamauchi. IBM – TDB introduces a CMOS inverter as a full swing output and a source follower as a partial swing output. IBM – TDB is the same as Taylor. IBM-TDB was cited to show a complementary source follower circuit but "does not show a back bias control circuit coupled to the back gate terminals of the transistors for controlling the threshold voltage of the transistors in active and standby modes." Also, in IBM-TDB there are no control connections from the back or body to the source or drain, which means there is a connection between source and body. Applicant's claims exclude a connection between the source and the body. IBM-TDB therefore seems to be equivalent to Dingwall and Taylor. Yamauchi

has been discussed. Applicant's comments made hereinabove concerning Yamauchi would apply equally well to this rejection.

Claim 8 was rejected under 35 U.S.C. 103(a) as unpatentable over IBM-TDB in view of Yamauchi. IBM-TDB and Yamauchi have been discussed hereinabove and Applicant has nothing further to add.

Claims 1 to 7, 9 to 18, and 21 were rejected under 35 U.S.C. 103(a) as unpatentable over Japanese '604 in view of Yamauchi. Taylor and Yamauchi have been discussed hereinabove and Applicant has nothing further to add. Japanese '604 was cited to show a complementary source follower circuit but "does not show a back bias control circuit coupled to the back gate terminals of the transistors for controlling the threshold voltage of the transistors in active and standby modes." Japanese '604 therefore seems to be equivalent to Dingwall, Taylor, and IBM-TDB. Yamauchi has been discussed. Applicant's comments made hereinabove concerning Yamauchi would apply equally well to this rejection.

Claim 8 was rejected under 35 U.S.C. 103(a) as unpatentable over Japanese '604 and Yamauchi. Japanese '604 and Yamauchi have been discussed hereinabove and Applicant has nothing further to add.

Applicant further notes, as to all the rejections, that the references cited to show a complementary source follower circuit already have improved methods for reducing power consumption. Nothing in those references suggests that the methods employed are inadequate. Therefore there is no motivation to combine the teachings of

Yamauchi with those references.

In Applicant's parent application, Applicant cited the paper "Impact of Die to Die and Within – Die Parameter Fluctuations ...", IEEE J.Solid – State Circuits, Vol. 37, No.2, Feb., 2002, pp.183 – 190. That paper states that in giga scale integration for future technology generation, process parameter fluctuations, such as in the threshold voltage, cannot be ignored. Applicant's invention addresses that problem. But in the cited art, there is no concern for that problem and no motivation to solve it.

All of the claims are now believed to be allowable over the references cited and reconsideration and allowance of all of the claims are therefore requested. Should the Examiner have other objections he is invited to call Applicant's attorney at (716) 774-0091 to resolve any remaining problems.

Respectfully,

Richard D. Fuerle
Registration No. 24,640
For Applicant

Richard D. Fuerle
1711 West River Road
Grand Island, NY 14072
(716)-774-0091
March 11, 2004
CASE YA03CIP